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ABSTRACT OF THE DISCLOSURE

A method of fabricating integrated circuitry comprises forming a conductive line having opposing sidewalls over a semiconductor substrate. An insulating layer is then deposited. The insulating layer is etched proximate the line along at least a portion of at least one sidewall of the line. An insulating spacer forming layer is then deposited over the substrate and the line. It is anisotropically etched to form an insulating sidewall spacer. A method of forming a local interconnect comprises forming at least two transistor gates over a semiconductor substrate. A local interconnect layer is deposited to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates. In one aspect, a conductivity enhancing impurity is implanted into the local interconnect layer in at least two implanting steps, with one of the implantings providing a peak implant location which is deeper into the layer than the other. Conductivity enhancing impurity is diffused from the local interconnect layer into semiconductor substrate material therebeneath. In one aspect, conductivity enhancing impurity is implanted through the local interconnect layer into semiconductor substrate material therebeneath. Field isolation material regions and active area regions are formed on a semiconductor substrate. A trench is etched into the field isolation material into a desired line configuration. A conductive material is deposited to at least partially fill the trench and form a conductive line therein.

Integrated circuitry is disclosed and claimed.